CLAIMS:

1. A method of multichannel analog/digital (A/D) conversion, in which in a first and second channel respectively in a first or second channel provision area a first and second analog signal awaiting conversion is sampled by a respective first and second S/H (Sample & Hold) element and the respectively stored sample value thereof is applied as a channel sample to a first and second input of an analog multiplexer for selection, wherein the processing of the respective channel sample then takes place in a processing cycle of all channels by said channel sample being selected in the analog multiplexer by a digital selection control signal for the analog/digital conversion and provided as analog selection signal at an output of the analog multiplexer and, after the respective channel provision area, being converted in an analog/digital converter, characterized in that aof the multichannel analog/digital conversion calculated in a channel controller (4) or defined by hardware by an expiry controller is valid for the respective entire channel including the detection of the channel sample in the first or second channel provision area (32), (35).

2. A method of multichannel analog/digital (A/D) conversion, in which in a first and second channel respectively in a first or second channel provision area a first and second analog signal awaiting conversion is sampled by a respective first and second S/H (Sample & Hold) element and the respectively stored sample value thereof is applied as a channel sample to a first and second input of an analog multiplexer for selection, wherein the processing of the respective channel sample then takes place in a processing cycle of all channels by said channel sample being selected in the analog multiplexer by a digital selection control signal for the analog/digital conversion and provided as analog selection signal at an output of the analog multiplexer and, after the respective channel provision area, being converted in an analog/digital converter, characterized in that an order of processing the channel sample detected in the respective first or second channel provision area (31, 35), which channel sample is provided by the analog selection signal (15) in an A/D conversion provision area (31) and then converted by the A/D converter, is calculated and determined individually for each channel sample by a channel controller (4).

3. A method as claimed in claim 2, characterized in that the calculations created in the channel controller (4) for the expiry of the multichannel analog/digital conversion are valid exclusively for detecting the channel samples in the first or second channel provision area (32, 35), wherein the detection of the channel sample present in the first or second channel provision area (32, 35) is respectively triggered by a first and second external detection signal (42, 41).

4. A method as claimed in claim 3, characterized in that a multichannel analog/digital conversion that continues through the detection of the channel sample present as analog signal in the first and/or second channel provision area (31, 35) is initiated in the A/D conversion provision area (31) by an external conversion request signal (40) which thus deposits a conversion request in the channel controller (4).

5. A method as claimed in claim 4, characterized in that additional data of the detected channel sample, which qualify an individual calculation of the time for processing a respectively detected channel sample in the channel controller (4), are notified to the channel controller (4) with the triggering of the conversion request by the additional external conversion request signal (40).

6. A method as claimed in claim 5, characterized in that the additional data, which are respectively notified to the channel controller (4) with the detected channel sample upon triggering of the associated conversion request signal (40), are an initial priority date, an increase rate of the priority per unit time, and an overall and a minimum validity period.

7. A method as claimed in claim 6, characterized in that the conversion request signals (40) are fed to the channel controller (4) together with the additional data on a data bus.

8. A method as claimed in any of claims 2 to 7, characterized in that the rules for individually calculating the time for processing a respectively detected channel sample are derived by means of metrics implemented in the channel controller.

9. A method as claimed in any of claims 2 to 8, characterized in that all signal-influencing times which lead to a shortening of the validity of a channel sample compared to

its individual sampling period within the first and/or second channel (36), (37) from the first and/or second S/H element (1), (2) to the A/D S/H element (5) upstream of the A/D converter (6) are combined to form an invalidity period and with their invalidity period form a configuration variable that influences the metrics.

10. A method as claimed in any of claims 2 to 9, characterized in that one configuration variable that influences the metrics is the residual validity of a channel sample.

11. A method as claimed in any of claims 2 to 10, characterized in that one configuration variable that influences the metrics is the minimum sampling period of a channel sample.

12. A method as claimed in any of claims 2 to 11, characterized in that the residual validity of a channel sample, which results from the currently remaining validity period of a respective channel sample present as analog signal in the respective assembly defining the analog signal, is determined in the form of a realized integrator assigned to this analog signal, wherein the integrator initial value which represents the validity period that has passed is presently monitored and, if this value exceeds the representing value of the overall validity (61), expiry of the validity period is ascertained, and otherwise its difference from the representing value of the overall validity (61) is the representing value of the remaining validity period.

13. A method as claimed in any of claims 2 to 12, characterized in that one configuration variable that influences the metrics is the randomly predefined priority of a channel sample.

14. A method as claimed in any of claims 2 to 13, characterized in that the respectively currently remaining validity period of the output signals of all the assemblies defining the analog signals in the first and second channel provision area (31, 35) is known to the channel controller (4) and the remaining validity period is continuously determined anew in advance, and in that the next signal processing step in the respective assembly defining the analog signal is thus triggered by the channel controller (4).

15. A method as claimed in any of claims 2 to 14, characterized in that in the case of expiry of the validity period of one of the output signals of the assemblies defining the analog signals being determined by the channel controller (4) in the first and second channel provision area (31, 35), an error signal (39) assigned to the respective output signal is output by the channel controller (4), or in the case of an available first S/H buffer memory or first further buffer memory (26, 43) or second S/H buffer memory or second further buffer memory (29, 44) these output signals are buffer-stored by means of a first buffer memory control signal (17a) or first further buffer memory control signal (17b) or second buffer memory control signal (16a) or second further buffer memory control signal (16b).

16. A method as claimed in any of claims 2 to 15, characterized in that one configuration variable that influences the metrics is the buffer-storage that has taken place of a channel sample in a first and/or second S/H intermediate element (26), (29) and/or a first and/or second further buffer memory (43), (44).

17. A method as claimed in claim 1, characterized in that the maximum conversion rate with which the analog selection signal (15) is A/D-converted in the A/D conversion provision area (31) is in a ratio V_i (i - channel index) to the respective detection rate of the first and second analog signal (11, 12) in the first and second channel provision area (32, 35), said ratio being respectively settable by the channel controller (4) and being averaged over the period of an overall processing cycle, in that this respectively averaged ratio V_1, V_2 is realized in the first and second channel (36), (37) by a control signal regime generated by the channel controller (4), wherein during the overall processing cycle, which is composed of successive processing part-cycles, the order and frequency of processing a respective channel sample of the first and second channel provision area (32, 35) is selected by this control signal regime in the processing part-cycles such that by means of the thereby set respective averaged ratio V_1, V_2 of the respective detection rate in the first and second channel (36, 37) to the maximum conversion rate during the period of the overall detection cycle in the A/D conversion provision area (31) it is ensured that the time required to detect the overall number of channel samples of the first and second analog signal (11), (12) detected within the first and second channel provision area (32, 35) with the respectively set detection rates is balanced out with the time required to A/D-convert all these values provided as analog selection signal (15) in the A/D conversion provision area (31), in that the channel controller (4) determines the value of the sum of the detection rates in the first and

second channel provision area (32), (35) and if it exceeds the value of the maximum conversion rate in the A/D conversion provision area (31) an error signal (39) is output, in that the detection of the first and second analog signal (11, 12) in each case takes place by memories in the first and second S/H element (1, 2), which is triggered by means of a first and second S/H control signal (17, 16) by the channel controller (4) with the respective detection rate, in that in order to provide the analog selection signal (15) the analog multiplexer (3) is actuated by the selection control signal (18) in accordance with the control signal regime of the channel controller (4), in that the subsequent A/D conversion of the analog selection signal (15) is carried out by actuating the A/D converter (6) with the A/D conversion signal (25), which in each case is carried out by the channel controller (4) in accordance with the control signal regime with the desired conversion rate.

18. A method as claimed in claim 17, characterized in that the respective average ratio V_i of the respective detection rate of the first and second analog signal (11, 12) in the first and second channel provision area (32), (35) to the maximum conversion rate of the analog selection signal (15) in the A/D conversion provision area (31) is characterized by the ratio:

V_i: ...: V_n (i - channel index, n - channel number)

with the subsidiary condition:

$$\sum_{i=1}^{n} U_i * V_i \leq 1$$

where: i - channel index 1, 2, ... i ... n (i is a natural number),

n - channel number (n is a natural number),

U_i - channel factor, with $U_i > 1$ (fractional number),

wherein with a channel factor greater than 1 the shortening of the validity of a channel sample is mapped in comparison to the sampling period, and in that optionally a buffer-storage of the first and second analog signal (11), (12) in the first and second channel provision area (32), (35) is carried out by means of a first and second S/H intermediate element (26), (29).

19. A method as claimed in claim 17 or 18, characterized in that the respective ratio of the respective detection rate of the first and second analog signal (11), (12) in the first and second channel provision area (32), (35) to the maximum conversion rate of the analog

selection signal (15) in the A/D conversion provision area (31) is binary-weighted and is characterized by the ratio equation:

V_i: ...: $V_n = 1/(2^i)$: ...: $1/(2^n)$

with the subsidiary condition:

$$\sum_{i=1}^{n} \frac{1}{2^i} \leq 1$$

where: i - channel index 1, 2, ... i ... n (i is a natural number), and

n - channel number, n > 1 (n is a natural number),

and in that optionally a buffer-storage of the first and second analog signal (11), (12) in the first and second channel provision area (32), (35) is carried out by means of a first and second S/H intermediate element (26), (29).

20. A method as claimed in any of claims 1 to 19, characterized in that within the A/D conversion provision area (31) a buffer-storage of the analog selection signal (15), triggered by the channel controller (4) by means of the A/D converter control signal (19), is carried out in the A/D sample & hold element (5), wherein the A/D converter sample (10) is provided at the output of the A/D sample & hold element (5) for subsequent A/D conversion in the A/D converter (6), and in that optionally a buffer-storage of the analog selection signal (15) is carried out by means of a first and second further buffer memory (43), (44).

21. A method as claimed in any of claims 1 to 20, characterized in that an output area (38) comprising the digital demultiplexer (7) and connected at least indirectly downstream of the A/D conversion provision area (31) comprising the analog/digital converter (6) at least indirectly provides at the respective outputs of the digital demultiplexer (7) the value converted for each channel by means of the demultiplexer selection signal (28) output by the channel controller (4), and in that these values are then buffer-stored in a first and second memory element (8), (9) assigned to the respective channel, said memory elements in each case likewise belonging to the output area, and read during activation of a respective first and second validity signal (23, 24).

22. A method as claimed in any of claims 1 to 21, characterized in that in times in which the assemblies contained in the A/D conversion provision area (31) and in the first and second channel provision area (32, 35) are not being used, wherein the analog/digital converter (6) is not performing any conversion and/or first and/or second S/H buffer

memories (26, 29) and/or first and/or second further buffer memories (43, 44) are not storing any channel samples (13, 14) or analog selection signals (15), these are placed in a state of low energy consumption so that the overall energy consumption is determined by the respective sampling ratios of the A/D conversion signal (25) and/or the first and/or second S/H buffer memory control signal (16a, 17a) and/or first and/or second further buffer memory control signal (16b, 17b).

23. A method as claimed in any of claims 1 to 22, characterized in that the multichannel analog/digital conversion takes place in the first and/or second channel (36, 37) and/or in a further channel (45), wherein the further channel (45) is actuated by the channel controller (4) by means of a supplementary control bus of the further channel (46).

24. A method as claimed in any of claims 1 to 23, characterized in that the first or second analog signal (11, 12) or a further analog signal (47) is input to the first and/or second channel (36, 37) and/or at least one further channel (45) for processing, wherein the channels that are multiple-occupied by an analog signal are actuated all differently or some differently by means of the associated external detection signals or S/H control signals.

25. An arrangement for multichannel analog/digital (A/D) conversion, wherein the arrangement samples, by means of a respective first and second S/H (Sample & Hold) element, in a first and second channel respectively in a first or second channel provision area a first and second analog signal awaiting conversion and applies the respectively stored sample value thereof as a channel sample to a first and second input of an analog multiplexer for selection, wherein the arrangement then processes the respective channel sample in a processing cycle of all channels by said channel sample being selected in the analog multiplexer by a digital selection control signal for the analog/digital conversion and provided as analog selection signal at an output of the analog multiplexer and, after the respective channel provision area, being converted in an analog/digital converter, characterized in that an expiry of the multichannel analog/digital conversion calculated in a channel controller (4) or defined by hardware by an expiry controller is valid for the respective entire channel including the detection of the channel sample in the first or second channel provision area (32), (35).

26. An arrangement for multichannel analog/digital (A/D) conversion, wherein the arrangement samples, by means of a respective first and second S/H (Sample & Hold) element, in a first and second channel respectively in a first or second channel provision area a first and second analog signal awaiting conversion and applies the respectively stored sample value thereof as a channel sample to a first and second input of an analog multiplexer for selection, wherein the arrangement then processes the respective channel sample in a processing cycle of all channels by said channel sample being selected in the analog multiplexer by a digital selection control signal for the analog/digital conversion and provided as analog selection signal at an output of the analog multiplexer and, after the respective channel provision area, being converted in an analog/digital converter, characterized in that an order of processing the channel sample detected in the respective first or second channel provision area (31, 35), which channel sample is provided by the analog selection signal (15) in an A/D conversion provision area (31) and then converted by the A/D converter, is calculated and determined individually for each channel sample by a channel controller (4).